REMARKS

Applicant is filing this amendment in further response to the outstanding Final Rejection dated November 7, 2003 and to the Advisory Action dated April 14, 2003. Concurrently herewith, applicant is also filing a Request for Continued Examination (RCE) application in compliance with 37 CFR 1.114, along with requesting an extension of time.

The Examiner continues to reject claims 1-8 under 35 USC 103(a) as being unpatentable over Ito, et al (U.S. Patent 6,333,206) in view of Urushima (JP 05-003183) and applicant's admitted prior art. Accordingly, applicant has amended claims 1 and 8 to overcome the outstanding rejection.

Applicant's invention is directed to a packaging process for a semiconductor package. First, a plurality of conductive bumps each having a flat end are formed on a chip-mounting area of a substrate. Next, a printing technique is used to form a first encapsulant for encapsulating the conductive bumps. This permits the top surface of the first encapsulant to be directly flush mounted with the flat ends of the conductive bumps and to form a coplanar surface in which the flat ends of the conductive bumps are exposed. Then, a chip is mounted on the coplanar surface, with bond pads on the chip being electrically connected to the exposed ends of the conductive bumps. The coplanar surface allows no gap to be formed between the chip and the first encapsulant, thereby not requiring a conventional gap-underfill process. Finally, a second encapsulant is formed to encapsulate the chip.

In Figures 6 and 7 of Ito, et al (U.S. Patent 6,333,206), there is a plurality of joint balls 2 formed on a printed circuit board 1 and encapsulated by a resin layer 13. Top portions of the joint balls 2 are exposed and protrude from the resin layer 13. Therefore, "Ito fails to teach or suggest conductive electrode portions having a flat end coplanar with the top of the first encapsulant" as claimed by applicant. In Figure 1 of Urushima (JP 05-003183), a plurality of bumps are formed on a semiconductor substrate 4 (i.e. chip) and encapsulated by a protective film 12 (epoxy resin). The protective film 12 is etched to reduce the thickness thereof and to expose flat ends of the bumps 10.

In the subject invention, the first encapsulant is printed directly on the top surface of the first surface flush with the flat ends of the conductive bumps, without any etching or grinding process needed to expose the bumps. This feature alone is not taught or suggested by either of the above cited references, solely or in combination, and makes the process of this invention simpler to implement.

Moreover, in Ito, et al, a heating process is performed to melt the resin layer 13 so as to fill the gap between the chip 3 and the molten resin layer 13. In Figure 2(a) of Urushima, the exposed bumps 10 on the chip 4 are connected to a plurality of protruded bumps 16 formed on the substrate 15, leaving a gap (not designated by a reference numeral) between the chip 4 and the substrate 15. If this gap is to be filled, and additional gap-filling process, e.g. conventional underfill technique, is required. Therefore, combining Ito, et al and Urushima still requires a gap-filling process to fill the gap between the chip and substrate. However, in the present invention, the chip is directly mounted on the coplanar surface formed by the first encapsulant and conductive bumps, without forming any gaps between the chip and the first encapsulant, and without

requiring any gap-filling process, thereby making the process of this invention distinguished over the cited references in combination.

For all the above reasons, the rejection of claims 1-8 under 35 USC 103 should be withdrawn.

Reconsideration and allowance of claims 1-8 is respectfully solicited.

Respectfully ~~submitted~~,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 8, 2003.

Date: May 8, 2003